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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/575,055 | 05/19/2000 | Q.Z. Liu | 99CON114P | 2945 |

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| EXAMINER | |
|---|---|
| LUU, CHUONG A | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2825 | |

DATE MAILED: 07/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/575,055 | LIU ET AL. | |
| | Examiner | Art Unit | |
| | Chuong A Luu | 2825 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,8-17 and 23* is/are rejected.

7)☒ Claim(s) *3-7 and 18-22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Arguments*

Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

The indicated finality of claims 1-23 is withdrawn in view of the newly discovered reference(s) to Tu et al. (U.S. 6,001,745), and Lee (U.S. 5,933,761). Rejections based on the newly cited reference(s) follow.

## PRIOR ART REJECTIONS

### Statutory Basis

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000.

Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**The Rejections**

Claims 1-2 and 16-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Tu et al. (U.S. 6,001,745).

Tu discloses a method for forming a via with

Respect to claims:

**(1)** covering a first area in a dielectric, said dielectric having a first dielectric constant;

exposing a second area in said dielectric to a dielectric conversion source so as to increase said first dielectric constant of said dielectric in said second area to a second dielectric constant (see column 3, lines 30-43);

**(2)** wherein said covering said dielectric with photoresist (see Figures 2C-2F);

**(16)** depositing a metal layer in a semiconductor die (see Figure 2A);

etching said metal layer to form a plurality of interconnect lines in a first area of said semiconductor die and a plurality of capacitor electrodes in a second area of said semiconductor die (see Figure 2A);

depositing a gap dielectric between said plurality of capacitor electrodes and between said plurality of interconnect lines (see Figure 2A);

covering said first area in said gap dielectric, said gap fill dielectric having a first dielectric constant (see Figure 2C);

exposing said second area in said gap dielectric to a dielectric conversion source so as to increase said first dielectric constant of said gap fill dielectric in said area to a second dielectric constant (see column 3, lines 30-43).

**(17)** wherein said covering step comprises covering said first area in said gap fill dielectric with photoresist (see Figure 2C).

Claims 8-10 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tu et al. (U.S. 6,001,745) in view of Lee (U.S. 5,933,761).

Tu teaches everything above except for further comprising steps of: etching a plurality of interconnect trenches in said first area in said dielectric and etching a plurality of capacitor trenches in said second area in said dielectric; further comprising a step of filling each of said plurality of capacitor trenches and each of said plurality of interconnect trenches with metal; wherein said metal is copper. However, Lee discloses a dual damascene structure with **(8)** further comprising steps of: etching a plurality of interconnect trenches in said first area in said dielectric and etching a plurality of

capacitor trenches in said second area in said dielectric (see Figure 3G); **(9)** further comprising a step of filling each of said plurality of capacitor trenches and each of said plurality of interconnect trenches with metal (see Figure 3H); **(10)** wherein said metal is copper (see column 4, lines 42-44); **(23)** wherein said metal layer comprises aluminum (see column 4, lines 42-44). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the above references to produce a semiconductor device to meet specific performance criteria.

Claims 11-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (U.S. 5,933,761) in view of Tu et al. (U.S. 6,001,745).

Lee discloses a dual damascene structure with

Respect to claims:

**(11)** forming a dielectric layer (302) in a semiconductor die, said dielectric layer having a first dielectric constant (see Figure 3A);

covering (304) a first area of said dielectric layer (302);

exposing a second area in said dielectric layer to a of said dielectric layer in said second area to a second dielectric constant (see Figures 3A-3B);

etching a plurality of interconnect trenches in said first area in said dielectric layer (see Figure 3G);

etching a plurality of capacitor trenches in said second area in said dielectric layer (see Figure 3G);

filling said plurality of interconnect trenches and said plurality of capacitor trenches with metal (see Figure 3H);

**(12)** further comprising a step of performing a chemical mechanical polish after said filling step (see column 4, lines 42-44);

**(13); (15)** wherein said metal is copper (see column 4, lines 42-44);

**(14)** forming a dielectric layer (302) in a semiconductor die, said dielectric layer having a first dielectric constant (see Figure 3A);

etching a plurality of interconnect trenches in a first area in said dielectric layer (see Figure 3G);

etching a plurality of capacitor trenches in a second area in said dielectric layer (see Figure 3G);

filling said plurality of interconnect trenches and said plurality of capacitor trenches with metal (see Figure 3G);

performing a chemical mechanical polish on said first and second areas (see column 4, lines 46-49);

exposing said second area in said dielectric layer to a said dielectric layer in said second area to a second dielectric constant (see Figure 3A);

Lee discloses the above outlined features except for wherein said dielectric conversion source comprises oxygen plasma. However, Tu discloses a method for forming a via with **(11); (14);** dielectric conversion source so as to increase said first dielectric constant of (see column 3, lines 30-43). It would have been obvious to one of

ordinary skill in the art at the time of the invention was made to combine the above references to produce a semiconductor device to meet specific performance criteria.

***Allowable Subject Matter***

Claims 3-7 and 18-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:30-3:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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July 26, 2004

CARIDAD EVERHART
PRIMARY EXAMINER